

Y. Shiga  
ADEKA CORP.



Naples, Italy  
June 4-8, 2006

PROCEEDINGS OF  
**The 18th International Symposium on  
Power Semiconductor Devices & ICs**

UNIVERSITY OF NAPLES FEDERICO II



# 4.5 kV 120A SICGT and Its PWM Three Phase Inverter Operation of 100kVA class

Y.Sugawara, Y.Miyanagi, K.Asano, A.Agarwal\*, S.Ryu\*, J.Palmour\*, Y.Shoji\*\*, S.Okada, S.Ogata, T.Izumi

Power Engineering R&D Center, Kansai Electric Power Co.,  
3-11-20 Nakoji, Amagasaki, 661-0974, Japan

\* CREE Inc., 4600 Silicon Dr., Durham, NC 27703, USA

\*\* ADEKA Co., 7-2-35 Higashi-ogu, Arakawa-ku, Tokyo, 116-8553, Japan

## ABSTRACT

4.5 kV 120 A SICGT with a chip size of 8 mm x 8 mm and a new high heat resistive resin capable of 400 °C operations were developed. The SICGT coated with the resin has a low leakage current of less than  $5 \times 10^{-6}$  A/cm<sup>2</sup> at both 4.5 kV and 250 °C, a low  $V_F$  of 5.0 V at 120 A, and short turn-on and turn-off times of 0.3  $\mu$ s and 1.7  $\mu$ s respectively.

A SICGT module was built by mounting one SICGT and two 6mm x 6mm SiC pn diodes in a metal can package, and a 110 kVA PWM 3 phase inverter was developed by using six of the SICGT modules. The electric power capabilities of both the developed SICGT and the 3 phase inverter are the largest ones among the reported SiC switching devices and SiC inverters, respectively.

## INTRODUCTION

In recent years, some high voltage SiC FETs demonstrated superior performance to those of Si devices [1,2]. However, due to a small chip area limited by crystal defects and a positive temperature dependence of  $R_{onS}$ , their current capabilities were small and the output powers of their 3 phase inverters were less than 7 kVA [3-5].

To achieve the large current capability in spite of the small chip area, some SiC-GTOs were developed [6,7] because they can exploit conductivity modulation and negative temperature dependence of  $V_F$  particular to bipolar devices. We have also developed 4.5 kV - 12.7 kV 4H-SiC SICGTs (SiC Commutated Gate turn-off Thyristors) [7,8], a 4 kVA SiC 3 phase PWM inverter and a 20 kVA half bridge inverter [7,9].

In this paper, both 4.5 kV 120 A SICGT and its PWM 3 phase inverter operations of 100 kVA class are presented.

## DEVICE DESIGN AND FABRICATION

### A. SICGT and Diode

Fig.1 shows a cross-sectional view of the developed SICGT. A p buffer layer was grown to reduce the excess carrier injection from the n<sup>+</sup> emitter, and an n<sup>+</sup> buried gate was introduced to reduce a storage time. SICGT has a low storage time, a low gate parasitic inductance, a low turn-off gain (less than 1) and a snubberless turn-off operation, which differentiates SICGT from SiC GTO. Because of these advantages, SICGT can achieve lower power losses than SiC GTO. In order to achieve the high blocking voltage, BV, a p<sup>+</sup> bases with low impurity concentration of  $1-2 \times 10^{14}$  cm<sup>-3</sup> and thickness of 75  $\mu$ m was used. Furthermore, a mesa JTE [10] is used as a termination structure, which was formed by ion implantations.

Fig.2 shows photographs of the developed SICGT chip. The chip size is 8mm x 8mm. The fabricated SICGT chips were mounted in the package, and electrical characteristics were measured. A gate electrode is formed between two anode electrodes. Three different types of emitter patterns were investigated for increase of the repetitive peak off-state current and the decrease of  $V_F$  etc.

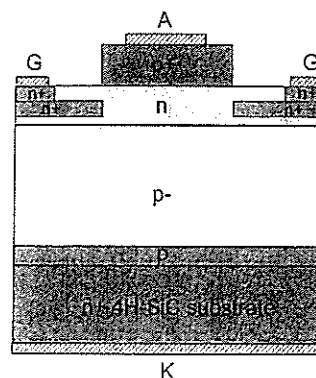


Fig.1. Cross-sectional view of SICGT.

In this paper, only the case of a simple stripe emitter shape is reported. 135 stripe emitters are formed under the each emitter electrode. Active area is about  $0.5 \text{ cm}^2$ .

### B. SICGT Module

By using one  $8 \text{ mm} \times 8 \text{ mm}$  SICGT and two  $6 \text{ mm} \times 6 \text{ mm}$  SiC diodes, one SICGT module shown in Fig.3 was fabricated, which has three terminals and a cap of about  $5 \text{ cm}$  in diameter and about  $2.5 \text{ cm}$  in height [7]. One of the diodes is a fly wheeling diode and the other is a energy release diode of an anode reactor. All SiC devices and wires are coated with an dielectric insulation resin to avoid discharges along the surface of SiC chips and between wires.

In order to achieve large current capability in spite of small chip size limited by various crystal defects, SICGT module has to be driven at high current density. Operation at high current density results in high device temperature. To operate SiC device at high temperature, for example at  $400^\circ\text{C}$ , not only the SiC devices but also both the package and the resin have to be high heat resistive.

The module package was improved for achieving high heat resistance, which was composed of copper alloy stem to reduce both an electric resistance and a thermal resistance. The stem and the cap are metallically coated to avoid an oxidation even at  $400^\circ\text{C}$  in an air atmosphere. BV of the package without SICGT and diode chips is confirmed to be more than  $7 \text{ kV}$ , which is measured as BV among the terminals and BV between the cap and the terminals in air.

To realize a high heat resistive module, a high heat resistive resin was also developed, which is called Nanotec-resin KA100 and can withstand high temperature of  $400^\circ\text{C}$ . Nanotec-resin KA100 is composed with one kind of polysiloxane and can be calcified by elevating its temperature but is soft like a rubber after calcifying. Conventional polysiloxane like silicon rubber is soft under about  $200^\circ\text{C}$ , but becomes solid above  $200^\circ\text{C}$  and many cracks generate within it because of its decomposition. This results in tremendous increase of the leakage current.

Nanotec-resin KA100, however, keeps the softness even at  $400^\circ\text{C}$ . Because the calcified Nanotec-resin KA100 has a three dimensional molecular network and a length of the molecular is arranged in several ten nanometers by using nano-technologies in order to make a thermal stress

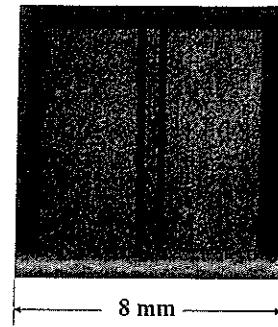
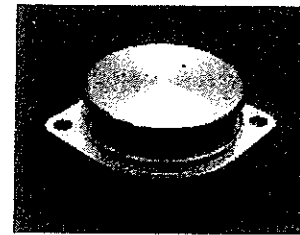
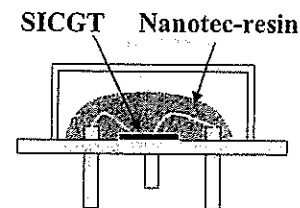


Fig.2. Photographs of developed SICGT chip.



(a) Photo.



(b) Cross-section

Fig.3. Package for module.

homogeneous at each molecular.

Therefore, SICGT coated with Nanotec-resin KA100 can operate at high current density and can handle large current in spite of its small chip area limited by crystal defects.

### ELECTRICAL CHARACTERISTICS

Fig.4 shows temperature dependence of the SICGT's off-state characteristics. The fabricated SICGT has high blocking voltage of more than  $5 \text{ kV}$ . Very low leakage currents of less than  $5 \times 10^{-6} \text{ A/cm}^2$  are realized even at both  $4.5 \text{ kV}$  and  $250^\circ\text{C}$ , which is less than  $1/10$  of that of  $6 \text{ mm} \times 6 \text{ mm}$  SiC diode [9] in spite of about 2 times active area. The excellent off-state characteristics is mainly caused to the high dielectric insulation of the developed Nanotec-resin KA100 and its high adhesion to materials composing the package.

Fig.5 shows on-state output characteristics of the SICGT. In spite of the small chip area of  $8 \text{ mm} \times 8 \text{ mm}$ , the large  $I_{AK}$  of more than  $200 \text{ A}$  is

achieved.  $V_F$  is less than 5.0 V at 120 A for temperature area of more than 100°C. A junction temperature of SICGT becomes greater than 100°C under PWM inverter operations.  $V_F$  of 5.0 V is almost equal to on-state rating voltages of commercialized 4.5 kV Si IGBTs, therefore,  $V_F$  of the developed SICGT becomes lower than those of the 4.5 kV Si IGBTs at higher temperature than 100°C.

Fig.6 shows its turn-off switching waveforms measured with an inductive load. The voltage after turning-off jumps to about 3.5 kV in spite of 2 kV supplied voltage due to the parasitic inductance of the circuits. But, a current of 250 A can be successfully turned off at a turn-off gain of about 1. A storage time, defined as a time between 0  $I_K$  and 0.9  $I_K$ , is about 1.46  $\mu$ s. A fall time, defined as a time between 0.9  $I_K$  and 0.1  $I_K$ , is about 0.24  $\mu$ s. A turn-off time is the sum of the storage time and the fall time and is 1.7  $\mu$ s. A turn-on time is short and is about 0.3  $\mu$ s. Because of the lower  $V_F$  and the higher switching speed, SICGT can be expected to realize a low power loss as compared to Si GTO and Si IGBT with the same rating blocking voltage.

### PWM THREE PHASE Inverter OPERATION

Fig. 7 shows a circuit of a PWM three phase inverter. The DC supply voltage was applied across the upper SICGT, the lower SICGT and their anode reactors connected in series in each phase. SiC has higher heat resistance than Si, and can withstand larger transient electric powers, therefore, the snubber circuits were not used for reduction of a switching power loss. Since the turn-on time of SICGT is very short, only anode reactors are used to reduce the abrupt current flow in the turn-on process of SICGTs thereby preventing device damage by localized heating. To generate PWM signals, a digital PWM control board was used, and these PWM signals were sent to gate drive circuits through optical fibers and were amplified to the current level needed for the turn-on and turn-off of SICGTs by the gate drive circuits which were mainly composed of Si MOSFETs. The dead time to avoid simultaneous current flow in two SICGTs is 10  $\mu$ s.

Fig.8 shows a fabricated three phase inverter, in which not only the PWM inverter circuits but also its power supplies and measurement tools are included. The PWM inverter circuit is composed with three stacks, each of which is corresponds to

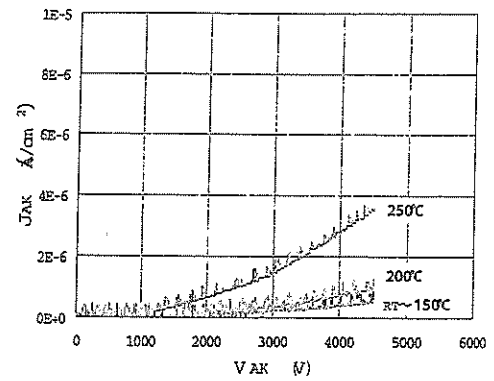


Fig.4. SICGT's off-state characteristics.

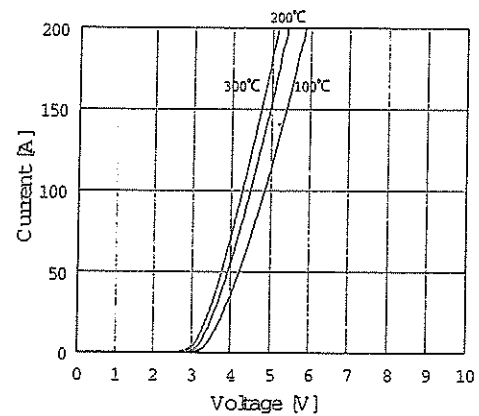


Fig.5. SICGT's on-state output characteristics.

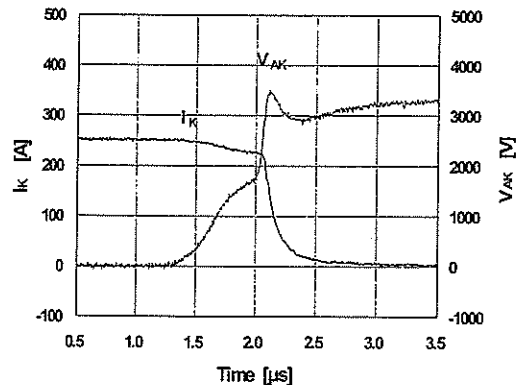


Fig.6. SICGT's turn-off switching waveforms.

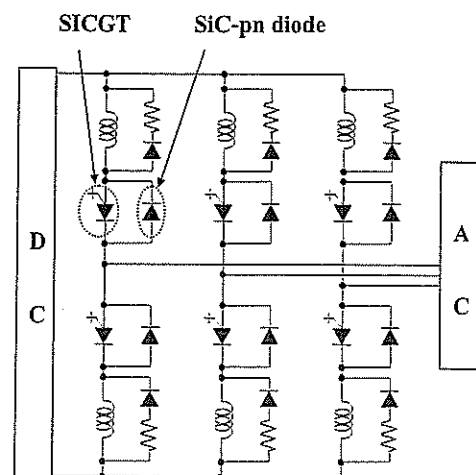


Fig.7. Main circuit of PWM three phase inverter.

one phase of the three phase inverter. One stack includes two sets of SICGT module, anode reactors, heat sinks, energy release resistors and gate drive circuits for each SICGT. The each SICGT module was attached to the each heat sink. Since the SICGT module can withstand the high temperature of greater than 250 °C, the heat sink can become compact and simple as compared with that of Si-IGBT inverter for the same electric power handling capability.

Fig.9 shows the output waveforms of the PWM 3 phase inverter. A carrier frequency is 2 kHz. The output voltage and the output current are ±1.9 kV and 98 A respectively. Since the voltage modulation ratio is 0.8, output power of 110 kVA is achieved, which is the largest output power among the reported SiC inverters.

Fig.10 shows progress in output powers of reported full SiC inverters [3-5,7]. The output power of 110 kVA is the largest one among them and is more than 15 times of those of SiC inverters reported by other companies previously.

### SUMMARY

4.5 kV 120 A SICGT with an 8 mm x 8 mm chip size and a new resin with high resistive temperature of 400 °C were developed. The SICGT coated with the resin has a low leakage current of less than  $5 \times 10^{-6}$  A/cm<sup>2</sup> at both 4.5 kV and 250 °C, a low  $V_F$  of 5.0 V at 120 A, and short turn-on and turn-off times of 0.3 μs and 1.7 μs respectively. Because of the high switching speed, SICGT can realize a low power loss as compared to commercial Si GTOs and Si IGBTs with the same rated blocking voltage.

A SICGT module was built by mounting the SICGT and two 6mm x 6mm SiC pn diodes in the metal can package, and a PWM 3 phase inverter with 110 kVA was developed by using six SICGT modules. The electric power capability of the developed 4.5 kV 120 A SICGT and 110 kVA 3 phase inverter are the largest ones among the reported SiC switching devices and SiC inverters, respectively.

### REFERENCES

- [1] Y.Sugawara, et al.: Proc. of ISPSD'01 (Toulouse), p.105 (2000).
- [2] K.Asano et al.: Proc. of ISPSD'02 (Santa Fe), p.61 (2002).
- [3] H.R.Chang et al. : Proc. of PESC'03, p.211 (2003).
- [4] J.H.Zhao et al.: Proc. of ICSCRM'03, vol.457, p.1137 (2003).
- [5] H.R.Chang et al. : Proc. of ISPSD'04 (Kitakyushu), p.351 (2004).

- [6] A.K.Agarwal et al.: Proc. of ICSCRM'01, vol.393, p.1349 (2001).
- [7] Y.Sugawara : Proc. of ISPSD'03 (Cambridge), p.10 (2003).
- [8] Y.Sugawara et al.: Proc. of ISPSD'04 (Kitakyushu), p.365 (2004).
- [9] Y.Sugawara : Proc. of ISPSD'05 (Santa Babara), p.295 (2005)
- [10] Y.Sugawara et al.: Proc. of ICSCRM'99, vol.338, p.1371 (1999).



Fig.8. Fabricated PWM 3 phase inverter.

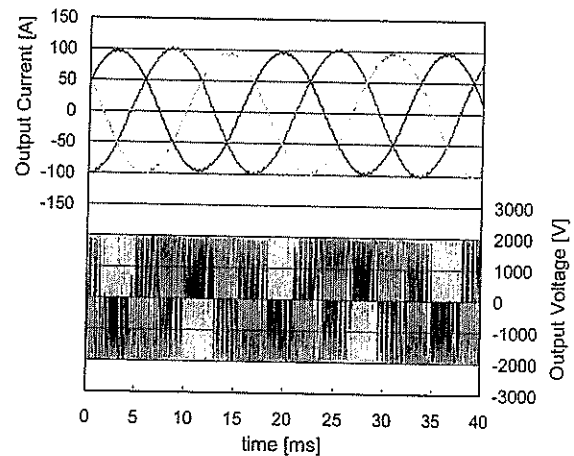


Fig.9. Output waveforms of PWM 3 phase inverter.

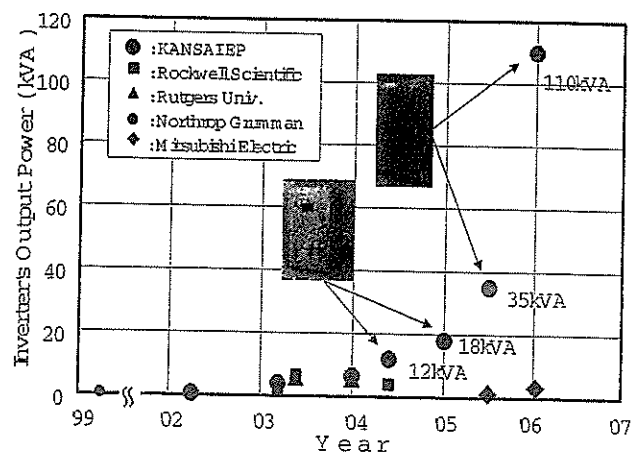


Fig.10. Progress in output powers of reported 3 phase SiC inverters.